US-PAT-NO: **6285865**

DOCUMENT-IDENTIFIER: US 6285865 B1

TITLE: System and method for on-chip filter tuning

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An integrated receiver with channel selection and image rejection substantially implemented on a single CMOS integrated circuit is described. A receiver front end provides programable attenuation and a programable gain low noise amplifier. Frequency conversion circuitry advantageously uses LC filters integrated onto the **substrate** in conjunction with image reject mixers to provide sufficient image frequency rejection. Filter tuning and inductor Q compensation over temperature are performed on chip. The filters utilize multi track spiral inductors. The filters are tuned using local oscillators to tune a substitute filter, and frequency scaling during filter component values to those of the filter being tuned. In conjunction with filtering, frequency planning provides additional image rejection. The advantageous choice of

local
oscillator signal generation methods on chip is by PLL out of band local oscillation and by direct synthesis for in band local oscillator. The VCOs in the PLLs are centered using a control circuit to center the tuning capacitance range. A differential crystal oscillator is advantageously used as a frequency reference. Differential signal transmission is advantageously used throughout
the receiver.

Within a receiver the layout and spacing of circuitry is critical to avoid the injection of noise generated in other portions of the circuit onto a received signal. If a tuner is placed on a semiconductor **substrate** noise generated in the **substrate** itself will interfere with, and degrade the received signal, this has been a problem preventing complete integration of a receiver on silicon.

Historically low noise substrates, fabricated from exotic and costly materials such as gallium arsenide have been used to reduce noise generated by the semiconductor **substrate**. However, it would be advantageous to be able to fabricate a receiver on a single CMOS **substrate**. CMOS advantageously is a known process that may be implemented economically for volume production.

Currently a receiver fabricated completely in CMOS has not been available without utilizing external components in the received signal path. Each time the signal is routed on or off of the integrated circuit additional opportunities for the introduction of noise into a signal path are provided. Minimizing this introduction of noise is an ongoing problem in receiver design.

In choosing intermediate frequencies for IF strips in the receiver, no concrete design guidelines exist. Also because of a wide variance in design goals that are encountered in receiver design, concrete methodologies do not exist. Each receiver must be uniquely engineered to satisfy a series of system design goals taking into consideration design tradeoffs that must be made. In the current state of the art, design tradeoffs, and design methodologies used have been directed to integrating all parts of the receiver except for frequencies selective components. The conventional wisdom in receiver design is that filters are not easily integrated onto a silicon **substrate** and that filtering is best done off of a chip.

An exemplary embodiment of the present invention utilizes a differential oscillator having low phase noise or jitter and high isolation, as a frequency reference that substantially increases the

performance of a tuner architecture integrated onto a single silicon **substrate**.

Remote (off chip) mounting of the crystal resonator requires that electrical contact between the crystal resonator and the associated oscillator circuit, be made with interconnecting leads of finite length. In integrated circuit technology, these interconnecting leads are typically implemented as circuit pads and conductive wires formed on a PC board **substrate** to which package leads are bonded (soldered) in order to effect electrical connection between the crystal resonator and an associated oscillator circuit. External electrical connections of this type are well known as being susceptible to noise and other forms of interference that might be radiated onto the interconnecting leads and, thence, into the oscillator circuit, degrading its overall noise performance.

FIG. 28 is a plan view of a multi-track spiral inductor. An inductor of this type is made from several long narrow strips of metal connect in parallel and disposed upon an integrated circuit **substrate**. A multi-track integrated spiral inductor tends to produce an inductance with a high Q. High Q is desirable to achieve lower noise floors, lower phase noise and when used in filters, a

better selectivity. To reduce series resistance and thus Q of a spiral inductor, wide track widths in the spiral are used. However, when track width is increased beyond 10-15 .mu.m the skin affect causes the series resistance of a spiral inductor to increase at high frequencies. Thus, Q is reduced even though a wide track has been used. This trend tends to limit the maximum Q achievable in integrated spiral inductors.

An exemplary embodiment of the invention utilizes a spiral inductor that is wound with several narrow tracks disposed in parallel upon a **substrate**. By splitting an exemplary 30 .mu.m wide track into two 15 .mu.m tracks disposed in parallel on the **substrate**, the inductor Q tends to increase. Alternative embodiments of the invention by utilize single track spiral inductors or multiple track inductors containing one or more tracks disposed in parallel upon a **substrate**. In the multiple track inductors described, the tracks are joined together at the beginning of a winding and again joined together at the end of the winding by a conductive material. An exemplary inductor suitable for integration is described in more detail in U.S. patent application Ser. No. 09/493,942 filed Jan. 28, 2000 entitled "Multi-Track Integrated Spiral Inductor" by James Yung-Chieh Chang; based

on U.S. Provisional Application No. 60/117,609 filed Jan. 28, 1999 (B600:34072) and U.S. Provisional Application No. 60/136,654 filed May 27, 1999 (B600:34676). The disclosure thereof is incorporated herein in its entirety by reference thereto.

It is a rule of thumb that the higher the frequency the smaller the dimensions of the integrated circuit component required in a filter to achieve a given set of circuit values. A spiral inductor of the type described in the embodiments of the invention allows an inductance to be satisfactorily fabricated on a CMOS **substrate**. Many alternative embodiments of the spiral are known to those skilled in the art. The realization of inductance required in any embodiment of the invention is not limited to a particular type of integrated inductor.

The overall effect of this is that when a device with high series resistance and thus, low Q is used as a component in a filter that the overall filter Q is low 2902. A high Q filter response is sharper 2984. The goal of a filter is to achieve frequency selectivity. The filter selectivity is the same electrical property as selectivity in the "front end" of the receiver previously described. If the filter has a low Q frequencies outside the pass

band of the filter will not achieve as great of an attenuation as if the filter contained high Q components. The high degree of selectivity is required to reject the multitude of undesirable distortion products present in a receiver that fall close to the tuned signal. Satisfactory inductor dimensions and device Q have been obstacles in integrating filters on a CMOS **substrate**.

Prediction of the inductance yielded by the spiral is closely approximated by formula. However, prediction of the inductor's Q is more difficult. Three mechanisms contribute to loss in a monolithically implemented inductor. The mechanisms are metal wire resistance, capacitive coupling to the **substrate**, and magnetic coupling to the **substrate**. Magnetic coupling becomes more significant in CMOS technologies with heavily doped substrates, because the effect of **substrate** resistance appears in parallel with the inductor. The first four or five turns at the center of the spiral inductor contribute little inductance and their removal helps to increase the Q. In spite of extensive research inductors implemented in CMOS possess Qs after limited to less than five.

In the exemplary embodiment the differential output 3506 advantageously tends

to provide noise rejection. In a differential output configuration, the signal at one terminal is 180.degree. out of phase from the signal at the other terminal and both signals are of substantially equal amplitude. Differential signals have the advantage that noise that is injected on either terminal tends to be canceled when the signal is converted back to a single ended signal. Such common mode noise is typically of equal amplitude on each pin and is typically caused by radiation into the circuit from external sources, or it is often generated in the circuit **substrate** itself. Advantageously, the present invention uses differential signal transmission at its output. It should be noted that in alternate embodiments of the invention, that a signal ended output can be produced from the differential signal by various techniques known in the art. Also, equivalently a differential input may be substituted for the single ended input shown.

After a channel is up conversion to a first IF 1918 of 1,200 MHz, it is next filtered by a bank of 3 LC band pass filters 1912 each having its response centered at 1,200 MHz in the embodiment. These filters in conjunction with the

second mixer 4802 provide 70 dB of image frequency rejection (4908 of FIG. 49). Filters are advantageously integrated onto the CMOS **substrate**. An LC filter comprises inductors (or coils) and capacitors. An inductor implemented on a CMOS **substrate** tends to have a low Q. The low Q has the effect of reducing the selectivity arid thus the attenuation of signals out of band.

The attenuation of signals out of band can be increased by cascading one or more filters. Cascading filters with identical response curves has the effect of increasing the selectivity, or further attenuating out of band signals. The embodiments of the invention advantageously incorporate active g.sub.m stage filters 1912,1934 to increase selectivity and provide circuit gain to boost in band signal strength. Three cascaded active LC filters implemented on a CMOS **substrate** yield a satisfactory in band gain, and provide approximately 35 dB of out of band image signal rejection in the embodiment described. However, the filters need not be limited to active LC filters, other characteristics and passive filters are contemplate equivalents.

Filters are available that will achieve a better rejection than an LC filter at a given frequency, for example a SAW

filter. While better filtering of the intermediate frequencies could be obtained with a filter such as a SAW filter at a higher frequency, a fully integrated receiver would not be achievable. A SAW filter is a piezoelectric device that converts an electrical signal to a mechanical vibration signal and then back to an electrical signal. Filtering is achieved through the interaction of signal transducers in the conversion process. A filter of this type is typically constructed on a zinc oxide (ZnO.sub.2), a material that is incompatible with integration on a CMOS circuit utilizing a silicon (Si) **substrate**. However in alternative embodiments of the invention, SAW or other filter types known in the art including external LC filters are contemplate embodiments. In particular, a hybrid construction utilizing receiver integrated circuit bonded to a hybrid **substrate** and filters disposed on the **substrate** is contemplated.

In generating the third LO signal of 231 MHz, typically a phase lock loop containing a voltage controlled oscillator would be used. However, these frequency components tend to be primary generators of spurious products that tend to be problematic. The present embodiments of the invention advantageously avoids the use of a PLL and

the attendant VCO in producing the third LO signal 1930 at 231 MHz. A divide by 4 circuit 4802 utilizes two flip-flops that create the I and Q third LO signals 1930 from the 925 MHz second LO 1904. This simple direct synthesis of the third LO tends to produce a clean signal. The reduced generation of distortion within the signal band tends to be important in an integrated circuit design where all components are in close physical proximity. If a PLL were used to generate the 231 MHz signal an external loop filter for the PLL would be utilized, providing another possible path for noise injection. By elegantly generating this third LO, that necessarily falls within the received signal bandwidth, noise and interference injection through the **substrate** into the received signal path tends to be minimized.

FIG. 52 shows a third alternate embodiment of the invention that tends to provide continuous tuning of the filter over temperature, and tends to more accurately keeps the response curve of the filter centered on the desired frequency. This embodiment of the invention preserves the separation of I 5202 and Q 5204 signals through the second IF stage 5206. In the third frequency conversion stage 5208 the I and Q signals are transformed into I', I, Q, and Q

signals. This alternate embodiment of the invention relies on a "three-stage poly phase" 5210 to provide image cancellation. The advantage of using a gyrator in place of dual LC filter bank 5212 is that a close relationship between I and Q tends to be maintained throughout the circuit. The phase relationship at the output of the gyrator filter tends to be very close to 90.degree.. If an LC filter is utilized there is no cross-coupling to maintain the phase relationship as in the gyrator. In the LC filter configuration complete reliance upon phase and amplitude matching is relied upon to maintain the I and Q signal integrity. The gyrator circuit has the additional advantage of tending to improve the phase relationship of signals initially presented to it that are not exactly in quadrature phase. For example, an I signal that is initially presented to the gyrator that is 80.degree. out of phase with its Q component has the phase relation continuously improved throughout the gyrator such that when the signals exit the gyrator quadrature phase of 90.degree. tends to be established between the I and Q signals, such as in a polyphase circuit element. This present embodiment of the invention provides the additional benefit of being easily integrated onto a CMOS **substrate** since the

gyrator eliminates the inductors that an LC filter would require. Filter timing and frequency generation utilize the methods previously described.

The frequency plan of this tuner allows it to be implemented in a single CMOS integrated circuit 4822 and functions as previously described in FIG. 48. This exemplary single up-conversion dual down conversion CATV tuner utilizes two PLLs that run off of a common 10 MHz crystal oscillator 5302. From the 10 MHz crystal oscillator references the PLLs generate two local oscillator signals that are used to mix down a received radio frequency to an intermediate frequency. This integrated CATV tuner advantageously uses differential signals throughout its architecture to achieve superior noise rejection and reduced phase noise. The receiver of the present invention advantageously provides channel selectivity and image rejection on the chip to minimize the noise injected into the received signal path. The differential configuration also tends to suppress noise generated on the CMOS **substrate** as well as external noise that is radiated into the differential leads of the 10 MHz crystal that connect it to the **substrate**. In this embodiment, an external front end as previously described is supplied on a

separate chip 5304 and an external filter 5306 is utilized.

a **substrate** upon which the electronic tuning circuitry is disposed;

20. The electronic tuning circuitry for tuning a filter of claim 19 wherein the **substrate** is silicon.

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TITLE: VIDEO SIGNAL PROCESSING DEVICE FOR EXTRACTING THE CHROMINANCE AND LUMINANCE SIGNALS FROM A COMPOSITE VIDEO SIGNAL IN A COLOR TELEVISION RECEIVER

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Furthermore, the luminance signal thus obtained tends to be attenuated in its high-frequency range of about 3.58 MHz .+-. 500 KHz, thus causing deterioration in the resolution and obscurity of the image. Such a disadvantage has been prevented by applying the output obtained from a carrier signal suppressing circuit to a variable response circuit comprising a **capacitor,** a resistor, and an inductance element for varying the response in a comparatively low frequency range (for instance, from 1 to 2 MHz) of the luminance signal, whereby a preshoot and an overshoot are provided on the luminance signal for improving the quality of the image.

In FIG. 4, there is indicated a signal wave

processing unit formed into a second order differentiating circuit which is employed for obtaining the signal shown in FIG. 2(b) from the video signal shown in FIG. 2(a). The differentiating circuit comprises transistors 903 and 910, bias resistors 901, 902, 908 and 909, and emitter resistors 904 and 911. The circuit further includes **capacitors** 905 and 906 which, together with the resistors 907 and 908 and 909, determine the input/output transfer function of this differentiating circuit. Furthermore, by selecting the constants of the transfer function suitably, a waveform as shown in FIG. 2(b) having a preshoot and an overshoot symmetrically arranged therein can be obtained, and the widths of these shoots can also be selected suitably.

US-PAT-NO: **4613828**

DOCUMENT-IDENTIFIER: US 4613828 A

TITLE: Injection-locked video frequency oscillator

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A pair of crystal-controlled oscillators 50 and 52 generate the clock signal provided to the clock drivers 28 and 40 and the color subcarrier signal provided to the encoder 44. The oscillator 50 includes a quartz crystal 54, which vibrates at a frequency of 10.738635 mHz, connected across an inverter 58 and a bias resistor 62. The oscillator's load **capacitance**, comprising fixed **capacitors** 66 and 67 and a variable **capacitor** 68, is distributed relative to both sides of the crystal 54 for increased stability. By adjusting the variable **capacitor** 68, the operating frequency of the oscillator 50 can be slightly varied. An additional inverter 74 "squares up" the oscillations from the inverter 58 and provides a square-wave output signal. The square-wave signal, which stems from the oscillator 50, is converted into a sine wave

(required for driving the delay lines) by a square-to-sine bandpass filter 80 having a frequency characteristic that sharply attenuates the higher harmonics of the square-wave signal. The sine-wave output signal from the bandpass filter 80 is provided to the clock drivers 28 and 40.

The oscillator 52 is configured similarly to the oscillator 50, excepting that it operates at a different frequency--one that is the fourth multiple of the subcarrier frequency--and includes a frequency divider 81 for obtaining the subcarrier frequency from the oscillation frequency. A quartz crystal 56, which vibrates at a frequency is of 14.31818 mHz, is connected across an inverter 60 and a bias resistor 64. The load **capacitors** include fixed **capacitors** 70 and 71, and a variable **capacitor** 72 for small frequency adjustments. An inverter 76 applies a square-wave oscillation signal to the divider 81. A pair of JK flip-flops 82 and 84 are connected as shown in the drawing to divide the incoming signal--applied to the clock input of the first flip-flop 82--by four. (The flip-flop pair can be obtained as a 74HC107 dual JK flip-flop with reset.)

A feedback connection 86 from the

divided-down output of the oscillator 52 (providing the color subcarrier signal) to the oscillator 50 (providing the clock signal) provides the solution to this problem. The feedback signal is the complement of the color subcarrier signal and is taken from the Q output port of the second flip-flop 84. This signal, being a square wave, is rich in odd harmonic content, including the third harmonic . . . which is nominally the same frequency as the clock signal. The third harmonic of the color subcarrier signal is separated by a series-resonant filter comprising an inductor 88 and a **capacitor** 90 and injected into the oscillator 50 at the input side of the inverter 58. When the oscillators are energized and the frequency of the injected signal begins to deviate from the oscillation frequency of the oscillator 50, the oscillation frequency will shift to the injected frequency. In other words, the phase of the oscillations will track the phase of the injected signal. The oscillator 50 is thus injection-locked to the third harmonic of the divided-down frequency from the oscillator 52. As circuit conditions change, the two frequencies (phases) will change with the conditions but they will always be locked to each other. By keeping the frequency (phase) of the oscillator 50 the same as the injected frequency, the clock signal will have a fixed and unvarying phase

relationship with the third harmonic of the color subcarrier signal present at the encoder 44. (The phase relationship can be other than a zero difference as long as the difference is fixed and unvarying.) The mixing problem in the video signal is thus eliminated and the accompanying low-frequency interference no longer shows in the reproduced picture.

One might be inclined to select values for the series-resonant filter (**capacitor** 90 and inductor 88) which produce resonance at the third harmonic of the color subcarrier signal. This has proven, however, to be an occasional problem in operating the oscillator 50 at the nominal frequency of the crystal 54 . . . probably because the oscillator 50 sees a low-impedance "short-circuit" at its resonant frequency. If the resonant frequency of the series-resonant circuit is offset a bit from the third harmonic so that the oscillator 50 does not see such low impedance, the oscillator 50 performs adequately. For example, a **capacitance** value of 12 pf. and an inductance value of 22 .mu.h were selected respectively for the **capacitor** 90 and the inductor 88 (a 10 pf. **capacitor** would have caused resonance at the third harmonic). It was however noted that other circuit **capacitances** influence this

"offset", and indeed may mask it entirely, so that a 10 pf. **capacitor** may function quite well when an actual oscillator circuit is assembled. In other words, the actual value of the components is an empirical determination based on the performance of the oscillator 50.